When hardware is free, power is expensive!

Is integrated power management the solution?

Michiel Steyaert, Filip Tavernier, Hans Meyvaert, Athanasios Sarafianos, Nicolas Butzen
KU Leuven ESAT-MICAS
Kasteelpark Arenberg 10, 3001 Leuven, Belgium
michiel.steyaert@esat.kuleuven.be

***Abstract*—In the last several years, significant efforts and advances have been made towards the CMOS integration of power converters. In this paper, an overview is given of what might be considered the next step in this domain: AC-DC conversion, efficient high-ratio voltage conversion, wide operating range and energy storage for energy scavenging. The main focus is on CMOS integration as this is the ultimate goal from any system integration point of view. Also, an overview of the state of the art will be discussed.**

I. Introduction

More and more, power management becomes a critical performance limitation in current and future state of the art electronic systems. For example, every building block in a System-On-Chip (SoC) requires its own supply voltage to operate optimally: a low voltage for the digital, a high voltage for the power amplifier and anything in between for other components. Tight regulation of all these supply voltages becomes a critical issue.

This challenge can best be solved by integrating the power management circuit on the same SoC. However, this typically means that it should be realized in a CMOS technology as that is the technology the SoC will most probably be realized in. This has been the topic of a previous paper [1].

In this paper, the question 'What is next?' will be addressed. This is important since in the domain of power conversion, one can take almost nothing for granted. For example, if a battery is used in an application, the power converter should be able to convert a decreasing input voltage from the battery into a stable output voltage. This problem is even more severe in the case of an application that takes its energy from discharging a capacitor. Guaranteeing a high efficiency over the full discharge cycle of this capacitor is a huge challenge which will be addressed here. Another example can be found in the interface between an application and the mains supply voltage. Traditionally, this is achieved by means of a big external power brick. The problem with this approach is that in a low-power state, i.e. standby mode, the efficiency of such a power brick is extremely bad as it is optimized for the full output power in active mode. Therefore, it makes sense to investigate the possibilities of an integrated power converter that directly interfaces with the mains voltage and makes the transformation from the high-voltage AC to the low-voltage DC in a very efficient manner. An onset to this challenge will be discussed in this paper.

This paper is organized as follows. In Section II, the principle and possible implementations of AC-DC conversion is discussed. In Section III, an overview is given of the available techniques to realize an efficient high voltage conversion ratio. Both semi-monolithic and monolithic approaches are presented. Section IV introduces converters with a wide operating range. The major problem in this regards is to enable a high efficiency over a wide range of input and output voltages. The challenges that are inherent in using energy scavenging are discussed in Section V. In Section VI, an overview of the current state of the art in the field of fully integrated power converters is presented. Finally, a conclusion is drawn in Section VII.

II. AC-DC Conversion

A. Why integrated AC-DC?

Research towards highly integrated mains AC to low voltage DC conversion can easily be justified. On the source side, the mains AC voltage is the predominant power distribution method toward the end user, and this on a global scale. On the electricity consumption side, voltage is required in a different form. Applications, which contain modern semiconductor integrated circuits, typically require a DC-voltage to operate. The actual voltage level varies depending on the specific application, but generally more recent integrated circuits require ever lower DC supply voltages. This leads to a large discrepancy in voltage specification between source and sink. Moreover, this discrepancy presents itself very often, which is proven by the multitude of AC-DC adaptors, wall warts or power bricks in a typical household.

Even though there is a positive evolution in AC-DC adaptors, they are not ideally suited to supply low power applications. A popular output power specification on the lower end of what is available for adaptors is 5V at 1A or 2A, resulting in 5W or 10W at the output, respectively. Below 10% of this nominal output power rating, high conversion efficiency can no longer be assumed in the adaptor. Consequently, such applications are better supplied by other mains AC-DC conversion approaches with better matching specifications.

This motivates the search for μW-level and mW-level solutions to bridge the voltage gap between source and sink, targeting low power applications. In the μW-range, possible application can be found in smart sensor networks, of which the terminology has evolved into the more popular and widely

accepted Internet-of-Things denomination. Alternatively, efficient delivery of mW-level output power can revolutionize standby power consumption of consumer electronic appliances by adding an auxiliary power supply. In addition, mW-level power supply from the mains can also serve as a main stand-alone solution for future low power target applications.

B. The AC-DC challenge: how to bridge the voltage gap

The mains AC as input to a converter presents challenging input voltage specifications up to 169V and 325V in case of the US and EU mains, respectively. The higher the intended level of CMOS integration, the more limited the options to interface such a high voltage become. This is a consequence of the limitation in voltage ratings of native CMOS integrated components, and the restriction to only use such components that yields fewer possible circuit implementations.

1) Active Devices: Standard nm processes typically offer switch voltage ratings of 2.5V/3.3V, which are already special-purpose Input-Output devices with higher ratings than the regular transistors standard in nm CMOS. Techniques such as stacking devices in series [2]-[3] can be used to construct switch blocks with enhanced voltage ratings, but are still limited by the finite body-to-substrate diode reverse breakdown voltage.

When larger switch blocking voltages are unavoidable, a possibility is to use a process with the option to implement lateral drain-extended MOS (LDMOS) devices. This enables active devices interfacing up to many ten's of volts.

2) Passive components: Passive components can on one hand be implemented with active devices in the case of a MOS-capacitor or with special process option components such as metal-insulator-metal (MIM) capacitors on the other hand. Unlike these passive components that are limited in voltage rating by the building blocks they are composed of, passive components implemented in the metal stack benefit from the freedom in layout to obtain custom designed voltage ratings. However, larger voltage ratings require larger spatial separation of the component terminals and thus result in a lower density of the integrated passive.

Next to full integration in a single stage, partitioning the mains AC-DC conversion over two cascaded stages allows increased design flexibility in each stage and enables each stage to focus more efficiently on a subset of the system challenges. This approach motivates to use external components to step-down the high voltage mains in a coarse manner to an intermediate voltage compatible with CMOS integrated active devices, which can then implement a secondary conversion and provide fine regulation of the output.

C. High input voltage architecture for monolithic AC-DC

A circuit solution to interface the mains in a monolithic approach must achieve a strict separation of the high voltages and the active devices. Fig. 1 shows a high input-voltage interface in which the high voltage is only seen over capacitor C_{in}, and only low voltage output V_{DC} is propagated to the active circuits to perform regulation.

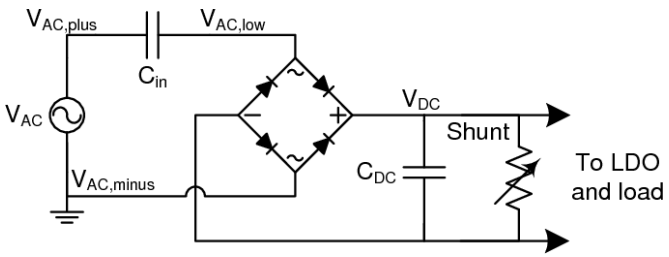

Fig. 1: Capacitive AC-DC step-down high voltage interface

However, having a series capacitor C_{in} to shield the actives from high voltage also results in a power throughput limitation, as the combination of a low capacitance value with the low mains frequency results in a large impedance. This causes only low currents through C_{in} to be realizable and consequently a low output power according to (1) and (2):

$$<|i_{Cin}|> = 4\, f_{mains}\, C_{in}\, (\sqrt{2}\, V_{AC} - V_{DC}) \quad (1)$$

$$P_{DC} = <|i_{Cin}|>\, V_{DC} \quad (2)$$

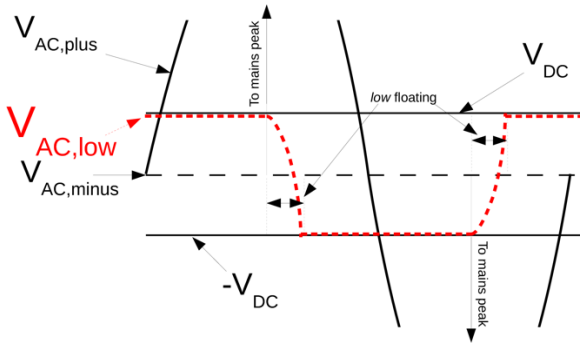

Fig. 2: Operational waveforms of capacitive AC-DC step-down interface

Fig. 2 shows the main waveforms during operation; assuming ideal diode forward voltages. The key feature in maximization of the power throughput in this interface circuit is the absence of a capacitive division in front of the rectifier, as implemented in [4]. As a result, $V_{AC,low}$ can be seen to show a block-pulse behavior with respect to $V_{AC,minus}$. This is an ideal input for the full-wave rectifier, which will conduct 91% and 93% in the demonstrator for US and EU mains inputs, respectively. In contrast, capacitive division of the mains [4], with the goal of dividing the mains to CMOS compatible values, causes $V_{AC,low}$ to be more sinusoidal and reduces rectifier conduction to 48% for a US mains input and consequently power throughput. However, the proposed optimal power throughput architecture of Fig. 1 depends on a nominal load current to be present in order for V_{DC} to remain within a safe operation range. Since this can not be expected of a load circuit, a shunt path is added internally to guarantee safe operation by ensuring the total current through the actual load and the shunt path is constant and equal to the nominal output current. For nominal power through the load, efficiency

is nominal, but at light load the efficiency is reduced due to the shunt path. Consequently, even though total power is in the lower uW's, the always-on use case is preferable for this mains AC-DC conversion approach.

The metal stack is used to build custom-rated high voltage passive components. Fig. 3 shows a half unit cell of capacitor C_{in}, in which the high voltage terminal is restricted to the top metal to achieve sufficient spacing to the substrate. On top of that, a 4µm spacing in between capacitor plates is required to enable a 400V breakdown rating [5]. Due to this large spatial separation, C_{in} capacitance density is limited to 12.5pF/mm2 and a total of 50pF was implemented.

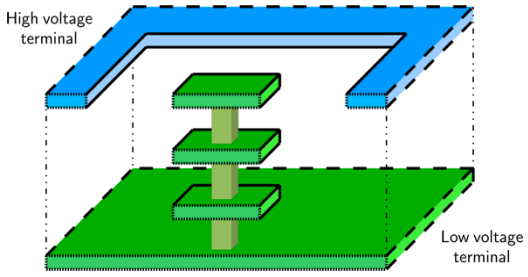

Fig. 3: Half unit cell of high voltage fringe capacitor conceptual cross section

In addition to a high voltage capacitor, a high voltage metal-stack resistor is introduced in between the input and C_{in}, not shown in Fig. 1. This resistor limits the inrush current, a current that occurs when applying the mains at a nonzero voltage instant to an uncharged capacitor, to a safe level. Implemented with the two highest metals and via's, 36kΩ is realized on an area of 0.28mm^2.

Fig. 4 shows the measured and calculated output power at a regulated 3.3V output as function of the mains input voltage. Output powers in the 4µW to 12µW range are possible with the reported approach, or 1.06µW/mm^2 to 1.58µW/mm^2 for a US and EU mains input, respectively. This is mainly limited by the die area cost of integrating a larger C_{in}.

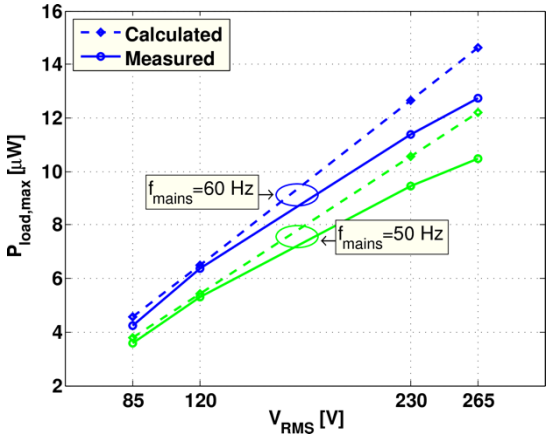

Fig. 4: Maximum output power for a regulated 3.3V output as function of mains specification, for a C_{in} of 50pF

In conclusion, the prototype of Fig. 5 enables µW-level output powers, but is not easily scalable toward higher output power levels, unless external components are used to allow for a larger C_{in} capacitance.

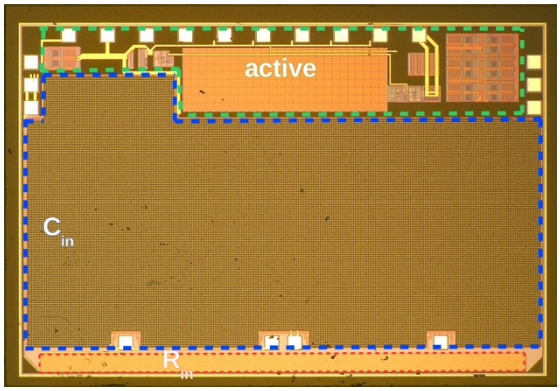

Fig. 5: Chip micrograph of monolithic AC-DC interface

D. Two-stage concept for compact and efficient low power from the mains

From the previous section, it has become clear that another approach is necessary to deliver mW-level power at low voltage from the mains. Instead of using external components to realize a larger power throughput according to (1) and (2), an entirely different approach is desirable to also eliminate shunt regulation and achieve high efficiency over a large load range.

In order to improve the system, a cascade of two individual stages is proposed, as introduced earlier. Hereby, the challenges of interfacing a high input mains voltage and delivering a low and tightly regulated output voltage can be more specifically optimized for in each block. Fig. 6 shows a mains conversion AC-DC concept consisting of two cascaded stages with an intermediate energy buffer.

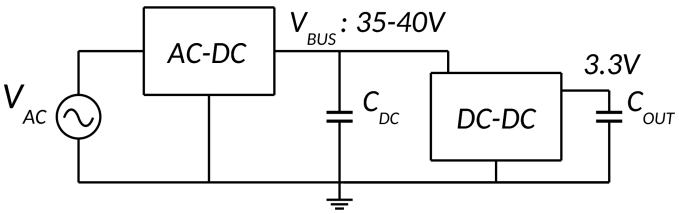

Fig. 6: Two-stage AC-DC conversion concept with intermediary buffer

In a first step, the mains AC is stepped down to and intermediate bus voltage at which energy is stored at a relatively high voltage, with respect to the output, to relax the C_{DC} capacitance specification. The selected voltage in the vicinity of 40V is selected as compromise between implementation efficiency and feasibility of the first and second stage. This stage focuses on handling high voltages and consequently requires external components that are rated

for this task. Regulation in this stage is of low priority and coarse regulation is intended to be sufficient.

Secondly, a highly integrated or even monolithic DC-DC converter can now focus on providing a clean regulated output voltage at high efficiency. To this end, the power of fast and flexible CMOS control circuits and regulation techniques can be unleashed without the burden of having to interface the mains directly. Even though the intermediate bus voltage is only a fraction of the mains, a Voltage Conversion Ratio (VCR) of more than ten is challenging at high conversion efficiency. Therefore, a more detailed discussion of implementations for the second stage follows in the next section.

III. Efficient High Voltage Conversion Ratio DC-DC

A. *Finding the architectural match*

Typical step-down is performed with the inductive buck converter, consisting of only two switches and one inductor. The VCR is set by the duty cycle of its Pulse-Width Modulation (PWM). For high conversion ratios, this leads to a very low duty cycle. With high switching frequencies being desirable to reduce the inductor size, the resulting on-time of the high-side switch becomes very short and significant driver losses are obtained by fast turn-on and turn-off of this full-input-voltage and current rated power switch.

Alternatively, Switched-Capacitor (SC) DC-DC converters rely on their topology structure to achieve a certain VCR and as such are optimized for a single ratio, while maintaining 50% duty cycle. Despite the larger component count, much lower voltage and current ratings are required of individual devices, which reduces conduction and driver losses. Consequently, SC DC-DC converters are promising candidates for high VCR.

The selection of a SC DC-DC approach still allows a lot of implementation flexibility. Unlike the fact that a certain SC topology leads to a single VCR, many topologies exist that realize the same single VCR. Two fundamental approaches appear as listed:

1) Semi-monolithic integration with external passives: External passive components allow for capacitance values orders of magnitude larger than monolithically feasible with standard processes, and this at higher Q factors. Consequently, semi-monolithic solutions can attain higher efficiency at higher output power level with respect to passive-limited full monolithic solutions. However, the amount of external components should be kept to a strict minimum in order to minimize the number of pins. This results in SC topologies that are very different from those suitable for monolithic integration, with its own set of specific design complexities.

2) Full monolithic integration: The context of monolithic integration poses other challenges than those of a semi-monolithic approach. Here, the limited capacitance values require higher operation frequency, which in turn increases the dynamic loss and negatively impacts the system efficiency. However, circuit techniques, such as fragmentation, become feasible as component count is no longer a limitation.

As discussed above, both approaches have their own merits and the following paragraphs report on the implementation of a semi-monolithic step-down SC DC-DC with a VCR of 11 on one hand and topology optimization towards a monolithic high VCR realization on the other hand.

B. *Semi-monolithic 11/1 SC DC-DC step-down converter with minimal external component count*

The minimal required number of flying capacitors to realize a certain VCR is theoretically derived in [6]. For a VCR range of 10-13, corresponding to target intermediate bus voltage values as in Fig. 6, a minimum of 5 flying capacitors is required by a 2-phase SC topology. Within the set of possible topologies that adhere to the minimum component requirement, the topology of Fig. 7 was found to be an ideal candidate as its power-switch driver requirements were the most relaxed of the compared topologies.

A transistor-level implementation of the SC topology is given in Fig. 7. The 16 switches are implemented with 3.3V thick-oxide transistors as well as lateral DMOS with a 20V V_{DS} rating. Switches S1-S8, shown in green, are closed during one topology phase while S9-S16, in blue, are open. Opposite open and closed switches form the other phase. Successive reconfiguration, with a 50% duty cycle, into the other phase results in charge transfer from input to output at a current multiplication of 11, i.e. a voltage step-down of 11. Each flying capacitor is implemented with a 25V rated 10µF 0603 ceramic surface-mount device.

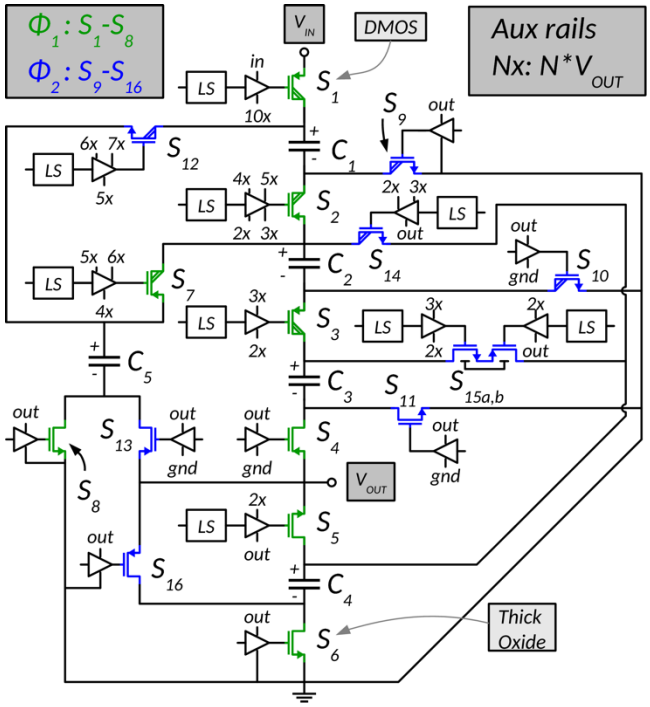

Fig. 7 : Transistor-level converter implementation, showing capacitors, power switches and power-switch drivers

Fig. 7 also details the auxiliary supply rails required by the power-switch drivers. Many of the integer DC levels between V_{out} and $11V_{out}=V_{in}$ are necessary to correctly drive this topology. The reason is that, while having a minimal capacitor count, the SC topology tends to have an irregular structure. A fully-integrated multiple-input multiple-output 11/1 ladder SC DC-DC converter was therefore implemented to provide these required auxiliary supply rails internally. Unlike the topology of Fig. 7, a ladder topology is a very regular structure with low voltage ratings for all switches and capacitors and thus a good match for CMOS integration. Hence, the higher component count of 22 switches and 21 capacitors is no issue.

With the availability of auxiliary power supply rails, correct operation of the custom power-switch drivers is no longer an issue and signal level translation can be performed by capacitive latch-based level shifters.

Fig. 8 shows the measured efficiency versus output power. A high efficiency across a broad output power range is achieved due to extensive Pulse Frequency Modulation. These results have been obtained for a regulated 3.3V output and input voltages in the 37.4V-39V range.

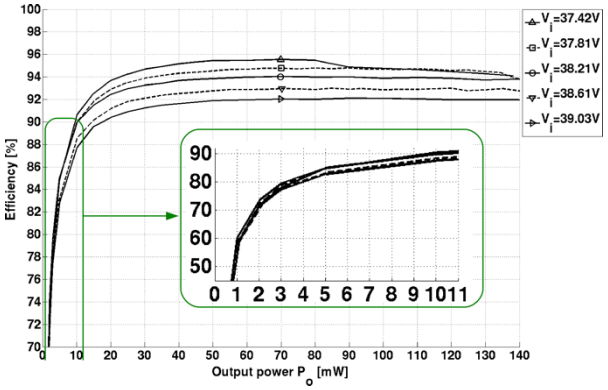

Fig. 8: Efficiency versus load power measurement for multiple input voltage and fixed 3.3V output

Fig. 9 shows the efficiency versus voltage conversion ratio. Although, as expected, inductive converters are able to convert a very wide range of VCR's, they fail to achieve both high efficiency and high voltage conversion ratio. Instead, the SC approach of Fig. 10 [7] can simultaneously realize high efficiency and high VCR, but for a narrow VCR range.

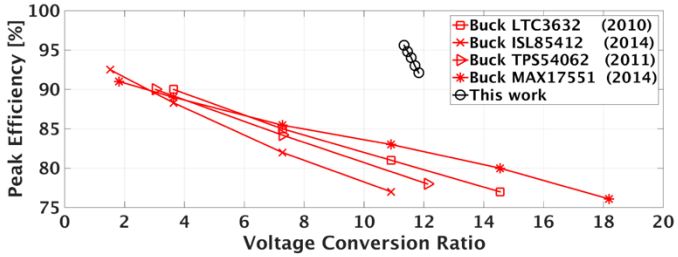

Fig. 9: Efficiency versus VCR comparison of the SC DC-DC to the state of the art

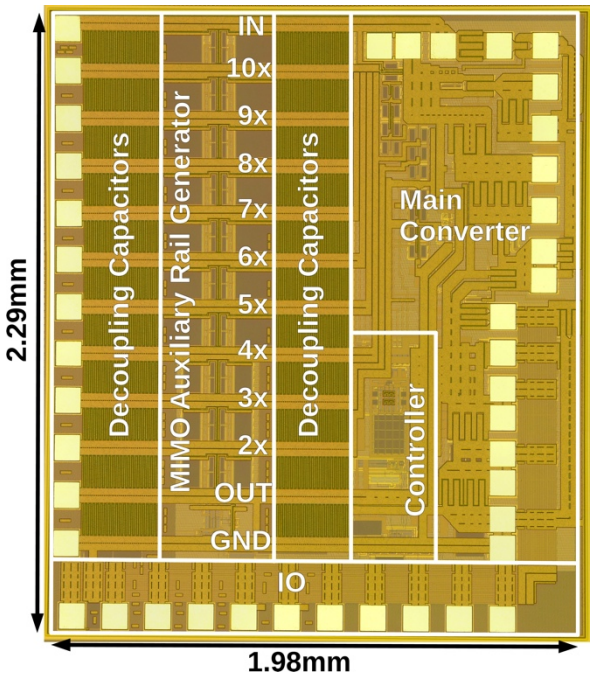

Fig. 10: Chip micrograph

C. Monolithic SC DC-DC towards very high VCR

SC DC-DC converters consist mainly of switches and capacitors, which are both readily available components in CMOS technology and thus enable monolithic integration. Consequently, they also heavily depend on the quality factor of these components. Unfortunately, integrated capacitors also exhibit parasitic capacitive coupling, which depending on the coupling factor and other capacitor-related system parameters, can translate into the dominant loss contribution [8]. Therefore, it is imperative to understand and quantify the mechanism in which SC DC-DC converters are affected by the parasitic coupling of their main energy storage and transfer element. Ultimately, the goal is to find and identify SC topologies that are least affected by this and thus form a good match for CMOS integration.

Not all integrated capacitors are alike, many capacitor implementations exist and each has its own advantages and drawbacks. Excluding exotic capacitor technologies, such as those with deep-trenches [9] and those with a ferro-electric dielectric [10], regular capacitors implementations include:

1) Gate-oxide: gate-oxide voltage rating limited; highest capacitance density; highest capacitive coupling

2) Metal-Insulator-Metal: double or triple voltage rating compared to gate-oxide capacitors; medium capacitance density; low capacitive coupling

3) Metal Fringing: highly customizable in all aspects; customizable voltage rating with inversely proportional capacitance density, but typically low; customizable capacitve coupling, but as well at the cost of capacitance density

In order to mitigate efficiency losses due to capacitive coupling of the flying capacitor to the substrate, two criteria emerge to quantify a SC DC-DC converter's susceptibility to this coupling:

1) Capacitor utilization efficiency: Not all SC topologies use the available capacitance resource optimally. Topologies that efficiently use the available capacitance, require less in total and therefore will end up with a lower absolute parasitic coupling value.

2) Parasitic coupling voltage swing: Charging and discharging a parasitic capacitor with a voltage source inevitably leads to losses. However, more energy is lost per charge-discharge cycle as the voltage difference between both states increases.

Table 1 combines topology-specific parameters in order to allow quantification and comparison of the susceptibility of the listed topologies. Only topologies known to have high capacitor utilization are compared. The capacitor utilization is represented by the K_c parameter in Table 1, where a lower number indicates a higher utilization efficiency. It can also be seen that this utilization efficiency increases with the VCR, which is denoted by parameter N in the table. However, convergence towards 1 is observed for all topologies, except the Doubler topology. Noting that a K_c value of 0.5 is obtained for a VCR of 2, it can be concluded that the capacitance overhead penalty of going from a low VCR of 2 toward a VCR of infinity is limited to a factor of only 2.

Within the set of these efficient capacitor-utilization topologies, Table 1 continues the comparison by listing the M_{sw} parameter, which is an aggregate value indicating the voltage swing seen by the parasitic capacitors in the topology. Again, a lower M_{sw} parameter indicates a lower voltage swing seen by the parasitic capacitors. Table 1 shows that increasing voltage conversion ratio N towards infinity also causes the M_{sw} parameter for all compared topologies, with the exception of the Dickson topology [11], also to quickly diverge towards infinity. Unlike the similarity in equally optimal capacitance utilization efficiency over all compared topologies, here a strong differentiation is observed. Table 1 clearly shows that the Dickson Star topology is the best candidate for high VCR DC-DC, in a monolithic context where parasitic coupling of the integrated capacitors can reduce system efficiency to the extent that monolithic integration is rendered infeasible.

IV. Wide Operating Range Converters

In many modern state-of-the-art SC DC-DC converters, it has become a de facto standard to combine multiple VCRs into a gearbox converter. These gearbox converters alleviate the biggest disadvantage of SC converters: the theoretical efficiency gamma=$V_{out}/(V_{in}*VCR)$ [12], which is the upper limit of the achievable efficiency.

SC converters can achieve high efficiencies for a given operating point (input and output voltage), but these efficiencies tend to degrade rather quickly when diverging from this operating point. By using multiple VCRs, efficiencies can be kept high over an increased input and/or output voltage range. However, compatibility of the different VCRs is essential, making it in most cases difficult to implement more than 2-3 ratios in one converter [13]. DAC-like techniques [14] can be used to substantially increase the number of VCRs, but these implementations target low power densities (<1mW/mm^2) with operating ranges limited to the V_{dd} of the used technology.

A well established SC topology, the so-called Dickson converter [11], has proven its merits in several applications

Table 1: Comparison of multiple capacitor-utilization efficient SC DC-DC topologies, focusing on parasitic coupling voltage swing toward high VCR

	Dickson Star	Series Parallel	Fibonacci	Dickson Star Embedded Cascade	Doubler
Fig. #	1(a)	1(b)	1(c)	1(d)	1(e)
# columns = k	$k = N-1$	$k = N-1$	$Fib_{k+2} = N$ [a]	$k = \frac{N}{2} - 1$ [b]	$k = 2log_2(N) - 1$
k_c	$[\frac{1}{N} \dots \frac{1}{N}]$	$[\frac{1}{N} \dots \frac{1}{N}]$	$[Fib_1 \dots Fib_k]$	$[\frac{1}{N} \dots \frac{1}{N}\ \frac{1}{4}\ \frac{1}{4}]$ [b]	$[\frac{1}{2}\ \frac{1}{2^2}\ \frac{1}{2^2}\ \frac{1}{2^3}\ \frac{1}{2^3} \dots \frac{1}{2^N}\ \frac{1}{2^N}]$
$V_{C,rated,i}$ $[V_{out}]$	[1 2 3 ... N-1]	[1 ... 1]	$[Fib_2 \dots Fib_{k+1}]$	[2 4 6 ... ($\frac{N}{2}-1$) 1 1] [b]	[1 2 2 4 4 ... $\frac{N}{2}\ \frac{N}{2}$]
$V_{sw,par,i}$ $[V_{out}]$	[1 ... 1]	[1 2 3 ... N-1]	$[Fib_1 \dots Fib_k]$	[2 ... 2 1 1] [b]	[1 2^1 0 2^2 0 ... $2^{log_2(N)}$ 0]
M_{sw}	$\frac{N-1}{N}$	$\frac{1}{N}\sum_{i=1}^{N-1} i^2$	$\frac{1}{N}\sum_{i=1}^{k}(Fib_i)^3$	$2.5 - \frac{4}{N}$	$\frac{1}{2} + \sum_{i=1}^{(log_2 N)-1} 2^{i-1}$
$K_c = (\sum_{i=1}^{N} \lvert k_{c,i} \rvert)^2$	$(\frac{N-1}{N})^2$				$(\frac{1}{2} + \sum_{i=1}^{(log_2 N)-1} 2^{-i})^2$
$K_c,\ N = \infty$	1				2.25
$M_{sw},\ N = 2$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$	$\frac{1}{2}$
$M_{sw},\ N = 4$	$\frac{3}{4}$	3.5	–	1.5	1.5
$M_{sw},\ N = 8$	$\frac{7}{8}$	17.5	4.62	2	3.5
$M_{sw},\ N = 16$	$\frac{15}{16}$	77.5	–	2.25	7.5
$M_{sw},\ N = 64$	$\frac{63}{64}$	1333.5	$N = 55 - 89$ 220.6 – 578	2.375	31.5
$M_{sw},\ N = \infty$	1	∞	∞	2.5	∞

[a] $Fib_1 = 1, Fib_2 = 1$ [b] $N > 2$ and N even and $\frac{N}{2}$ even

where a boosted voltage is required. Increasing the boosted voltage is simply done by adding an extra unit cell in the cascade, where N stages lead (for a capacitive load) to an output voltage of V_{in}*(N+1). The Dickson converter can also be used as a step-down converter, as in Fig. 11. Interestingly, by simply changing the turn-on phases of the power train switches, flying capacitors can be merged, emulating a new VCR. In this way, an N stage Dickson step-down converter can not only perform (N+1):1 division, but also a 1, 2, …, N division, without any additional power train switches or flying capacitors required. In Fig. 11, it is shown how the same step-down converter can go from a 5:1 VCR to a 3:1 VCR.

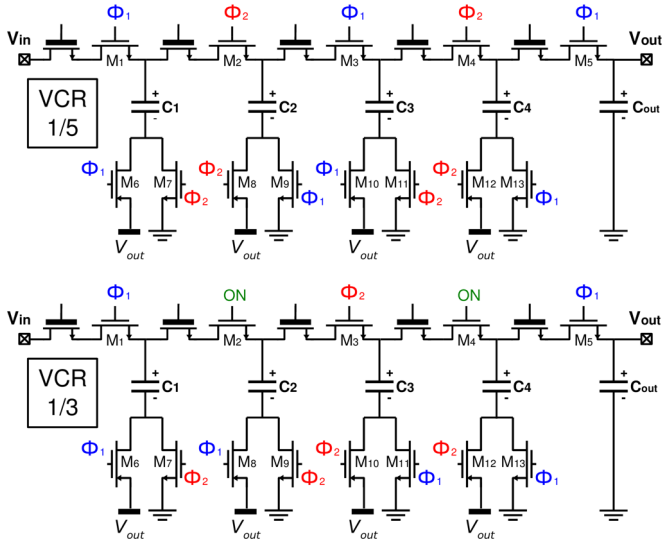

Fig. 11: Example operation of the folding Dickson converter in 1/3- and 1/5-mode

As a proof of concept, a four-stage folding Dickson converter has been designed and fabricated in a 90nm technology. Special care had to be taken to drive switches $M_{1\text{-}4}$, since their drain and source voltages vary widely depending on input voltage and VCR. This motivated the choice to implement dedicated converters for each switch, generating a low power supply voltage referenced to the source of the switch.

The four VCRs (2:1, 3:1, 4:1 and 5:1) allow a safe input voltage operating range (i.e. without violating the maximum drain-source voltage allowed over the power train switches) from 2.8V up to 8V (>$4V_{dd}$), delivering up to 50mW of output power at 1.2V. Measurements have been performed down to 5mW of output power.

Fig. 12 shows the attained efficiency for an output power of 32mW. Peak efficiencies up to 77% have been recorded, while average efficiencies above 60% are achieved over the measured output power range. This graph also compares the measured input current of the converter with the input current of an idealized DC-DC converter with a fixed efficiency and output power. In the case of the folding Dickson converter, the actual input current is a staircase approximation of this idealized current. Increasing the input voltage resolution of the converter, i.e. increase the amount of VCRs over the same input voltage range, would lead to a much better approximation

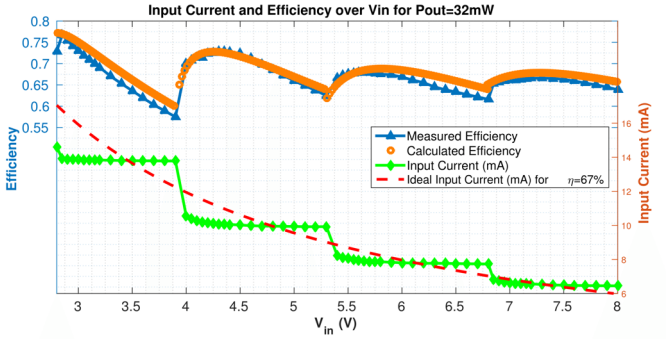

Fig. 12: Input current and efficiency as a function of input voltage

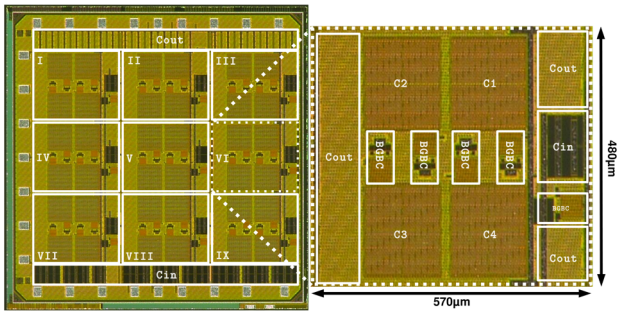

Fig. 13: Chip photograph of the fabricated design

of this input current, the ultimate goal of SC gearbox DC-DC converters.

Fig. 13 shows the chip photograph of the design, processed in a 90nm technology, and a detail of one of the nine fragments.

V. Energy Storage for Energy Scavenging

Although energy scavenging greatly reduces the need for large and bulky batteries, it does not eliminate energy storage entirely. The energy storage remains a vital element in any system that relies on scavenged energy, either as a buffer to account for fluctuations in the harvested energy, or as an accumulator to allow more power hungry applications to be activated every time enough energy has been collected.

Most energy scavenging systems therefore still require batteries, simply because they are able to provide the necessary capacity. However, when considering the further miniaturization of these systems, the large form factor of even the smallest batteries poses a serious problem and there are consequently many ongoing efforts to increase their level of integration.

Fabricating Thin-Film batteries on top of integrated circuits (IC) could be one of the solutions, but still many hurdles need to be overcome [15]. They have a reduced energy density and more severe capacity degradation over charge/discharge cycles compared to their discrete counterparts. Furthermore, because of their smaller size, their internal resistance is much larger, drastically limiting the amount of current that can be drawn from them.

An alternative is a 3D, Deep-Trench (DT) battery fabricated with Reactive Ion Etching (RIE) [16]. Thanks to the extra dimension, their energy density could be much higher. Moreover, research has shown they could be fabricated in such a way that their capacity does not degrade. Although promising, an integrated implementation has yet to be reported.

Instead of trying to make batteries smaller, it is also possible to use capacitors which are native to any CMOS technology. Integrated capacitors, whether Metal-Oxide-Semiconductor (MOS), Metal-Oxide-Metal (MOM) or Metal-Insulator-Metal (MIM), have a much lower internal resistance and no noteworthy capacity degradation. Their energy density is not as high as those of batteries, but they do have the advantage of benefiting automatically from technology scaling. The energy density of a capacitor also depends on its voltage squared, which means that by allowing higher voltages, their density could be significantly improved.

Contrary to their battery counterpart, DT capacitors have been successfully fabricated [17] and integrated with other circuits [18]-[21]. These capacitors are able to provide energy densities of up to two orders of magnitude larger, which might make them the energy storage of choice of the future.

VI. State of the Art Comparison

In Fig. 14, the current state of the art for fully integrated SC converters is shown.

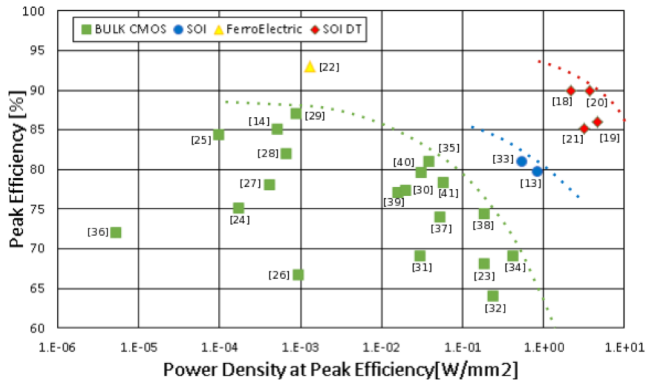

Fig. 14: State of the art of fully integrated capacitive DC-DC converters

Each of the four different technologies has a distinct position on the spectrum. Bulk CMOS converters have been the most frequently reported and have been used for a large range of power levels. Consequently a clear trade-of between power density and efficiency can be seen at higher power densities. In theory, the efficiency should saturate and reach a maximum value determined by the parasitic substrate coupling at lower power densities [13], but there is no sign of it in reported converters. In fact, there seems to be a positive slope at these power levels. Leakage and control overhead, both factors which are often excluded in models, might be the cause for this.

SOI converters have a power density advantage over bulk CMOS converters because of their reduced transistor parasitics. Combined with DT capacitors, the gap gets even larger. Thanks to their significantly higher capacitor density, the frequency of the converter can be two orders of magnitude lower for the same power density. Furthermore, the coupling to the substrate does not increase with the same factor, leading to an additional efficiency advantage. One design has used Ferro-Electric capacitors which, like the DT capacitors, have higher capacitance density and significantly lower parasitic coupling to the substrate. The latter has resulted in a record fully integrated efficiency of 93% [22].

Overall, while bulk CMOS does a good job at providing integrated power conversion for low to medium power levels, it is clear that ultimately the capacitor, both in terms of density and parasitics, remains the largest bottleneck. More exotic technologies, improving on both points, consequently see a significant improvement and have been shown to be viable for high power applications [21].

VII. Conclusion

This paper has given an overview of the current research that is being done in the domain of integrated power conversion. Besides the integration of SC DC-DC converters which is already well understood, the next challenges have been tackled: AC-DC conversion, efficient high voltage conversion, wide operating range and energy scavenging solutions. The broad state of the art overview of integrated power converters is a showcase of this well established but also very exciting research domain.

VIII. Acknowledgements

Many thanks to Infineon, NXP, FWO and IWT for the technical discussions and the financial support.

References

[1] Steyaert, M.; Van Breussegem, T.; Meyvaert, H.; Callemeyn, P.; Wens, M., "DC-DC converters: From discrete towards fully integrated CMOS," *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, pp.42,49, 12-16 Sept. 2011

[2] A.-J. Annema, G. J. G. M. Geelen, and P. C. de Jong, "5.5-V I/O in a 2.5-V 0.25um CMOS technology," IEEE Journal of Solid-State Circuits, vol. 36, no. 3, pp. 528–538, 2001

[3] B. Serneels, T. Piessens, M. Steyaert, and W. Dehaene, "A high-voltage output driver in a 2.5-v 0.25-um cmos technology," IEEE Journal of Solid-State Circuits, vol. 40, no. 3, pp. 576–583, 2005

[4] A. A. Tamez, J. A. Fredenburg, and M. P. Flynn, "An integrated 120 volt ac mains voltage interface in standard 130 nm cmos," in Proc. ESSCIRC, 2010, pp. 238–241

[5] Timedomain CVD Inc. silicon dioxide : Properties and applications. [Online]. Available: http://www.timedomaincvd.com/CVD Fundamentals/films/SiO2 properties.html/

[6] M. S. Makowski and D. Maksimovic, "Performance Limits of Switched-Capacitor DC-DC Converters," in Proc. IEEE Power Electronics Specialists Conf. (PESC), vol. 2, 1995, pp. 1215–1221

[7] H. Meyvaert, G. Villar Piqué, R. Karadi, H. J. Bergveld, and M. Steyaert, "A Light-Load-Efficient 11/1 Switched-Capacitor DC-DC Converter with 94.7% Efficiency While Delivering 100mW at 3.3V," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2015 IEEE International, 2015, pp. 358–359

[8] H. Meyvaert, A. Sarafianos, N. Butzen and M. Steyaert, "Monolithic switched-capacitor DC-DC towards high voltage conversion ratios," Control and Modeling for Power Electronics (COMPEL), 2014 IEEE 15th Workshop on , pp.1,5, 22-25 June 2014

[9] G. Wang et al., "Scaling deep trench based eDRAM on SOI to 32nm and Beyond," in Electron Devices Meeting (IEDM), 2009 IEEE International, Dec 2009, pp. 1–4

[10] Rodriguez et al., "Reliability of ferroelectric random access memory embedded within 130nm cmos," in Reliability Physics Symposium (IRPS), 2010 IEEE International, May 2010, pp. 750–758

[11] Dickson, J.F., "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," Solid-State Circuits, IEEE Journal of , vol.11, no.3, pp.374,378, Jun 1976

[12] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC-DC Converters," IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 841–851, 2008.

[13] Hanh-Phuc Le; Sanders, S.R.; Alon, E., "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," Solid-State Circuits, IEEE Journal of , vol.46, no.9, pp.2120,2131, Sept. 2011

[14] Salem, L.G.; Mercier, P.P., "An 85%-efficiency fully integrated 15-ratio recursive switched-capacitor DC-DC converter with 0.1-to-2.2V output voltage range," Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, pp.88,89, 9-13 Feb. 2014

[15] J.F. Ribeiro, R. Sousa, J.A. Sousa, L.M. Goncalves, M.M. Silva, L. Dupont and J.H. Correia, "Flexible Thin-Film Rechargeable Lithium Battery," in *Proc. Transducers & Eurosensors XXVII 17th Conf. Solid-State Sensors, Actuators and Microsystems*, June 16-20, 2013, pp.2233-2236

[16] P.H.L. Notten, F. Roozeboom, R.A.H. Niessen and L. Bagetto, "3-D Integrated All-Solid-State Rechargeable Batteries," *Advanced Materials*, vol. 19, no. 24, pp. 4564-4567, Dec. 2007

[17] B. Jayaraman, S. Gupta, Y. Zhang, P. Goyal, H. Ho, R. Krishnan, S. Fang, S. Lee, D. Daley, K. McStay, B. Wunder, J. Barth, S. Deshpande, P. Parries, P. Malik, P. Agnello, S. Stiffler and S. S. Iyer, "Performance analysis and modeling of deep trench decoupling capacitor for 32 nm high-performance SOI processors and beyond," in *Proc. IEEE Int. Conf. IC Design Technol*., pp. 1-4, 2012

[18] C. Leland , R. K. Montoye , B. L. Ji , A. J. Weger , K. G. Stawiasz and R. H. Dennard, "A fully-integrated switched-capacitor 2:1 voltage converter with regulation capability and 90% efficiency at 2.3A/mm2 ," in *Proc. IEEE Symposium VLSI Circuits*, June 16-18, 2010, pp. 55-56

[19] T. M. Andersen, F. Krismer, J.W. Kolar *et al.*, "A 4.6W/mm2 power density 86% efficiency on-chip switched capacitor DC-DC converter in 32 nm SOI CMOS," in *Proc. IEEE 28th APEC*, March 17-21, 2013, pp. 692-699

[20] T. M. Andersen, F. Krismer, J. W. Kolar, T. Toifl, C. Menolfi, L. Kull, T. Morf, M. Kossel, M. Brändli, P. Buchmann and P. A. Francese, "A sub-ns response on-chip switched-capacitor DC-DC voltage regulator delivering 3.7W/mm2 at 90% efficiency using deep-trench capacitors in 32nm SOI CMOS," in *IEEE ISSCC 2014 Digest of Technical Papers*, February 9-13, 2014, pp. 90-91

[21] T. M. Andersen, F. Krismer, J.W. Kolar *et al.*, "A Feedforward Controlled On-Chip Switched-Capacitor Voltage Regulator Delivering 10W in 32nm SOI CMOS," in *IEEE ISSCC 2015 Digest of Technical Papers*, February 22-26, 2015

[22] D. El-Damak, S. Bandyopadhyay, and A.P. Chandrakasan, "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors," *IEEE ISSCC 2013 Digest of Technical Papers*, February 17-21, 2013, pp. 374-375

[23] D. Maksimović and S. Dhar, "Switched-Capacitor DC-DC Converters for Low-Power On-Chip Applications," in *Proc. IEEE Power Electronics Specialists Conf. (PESC) 1990*, 1990, vol. 1, pp 54-59

[24] Y.K. Ramadass and A.P. Chandrakasan, "Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications," in *Proc. IEEE Power Electronics Specialists Conf. (PESC) 2007*, June 17-21, 2007, pp 2353-2359

[25] M. D. Seeman , S. R. Sanders and J. M. Rabaey, "An ultra-low-power power management IC for energy-scavenged Wireless Sensor Nodes," in *Proc. IEEE Power Electronics Specialists Conf. (PESC) 2008*, June 15-19, 2008, pp 925-931

[26] S. Ling, M. Dongsheng and A.P. Brokaw, "A Monolithic Step-Down SC Power Converter with Frequency-Programmable Subthreshold z-Domain DPWM Control for Ultra-Low Power Microsystems, " in *Proc. European Solid-State Circuits Conf. (ESSCIRC) 2008*, Sept. 16-19, 2008, pp. 58-61

[27] J. Kwong , Y. K. Ramadass , N. Verma and A. P. Chandrakasan, "A 65 nm Sub-Vt Microcontroller With Integrated SRAM and Switched Capacitor DC-DC Converter," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 115-126, Jan. 2009

[28] T. Van Breussegem and M. Steyaert, "A 82% Efficiency 0.5% Ripple 16-Phase Fully Integrated Capacitive Voltage Doubler," in *Proc. IEEE Symposium VLSI Circuits*, June 16-18, 2009, pp. 198-199

[29] T. Van Breussegem and M. Steyaert, "A fully integrated gearbox capacitive DC/DC-converter in 90nm CMOS: Optimization, control and measurements," in *Proc. Workshop on Control and Modeling for Power Electronics (COMPEL) 2010*, June 28-30, 2010

[30] T. Van Breussegem and M. Steyaert, "A fully integrated 74% efficiency 3.6V to 1.5V 150mW capacitive point-of-load DC/DC-converter," in *Proc. European Solid-State Circuits Conf. (ESSCIRC) 2010*, Sept. 14-16, 2010, pp. 434-437

[31] Y. K. Ramadass , A. A. Fayed and A. P. Chandrakasan, "A Fully-Integrated Switched-Capacitor Step-Down DC-DC Converter With Digital Capacitance Modulation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557-2565, Dec. 2010

[32] D. Somasekhar , B. Srinivasan , G. Pandya , F. Hamzaoglu , M. Khellah , T. Karnik and K. Zhang, "Multi-Phase 1 GHz Voltage Doubler Charge Pump in 32 nm Logic Process," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 751-758, April 2010

[33] H. P. Le , M. Seeman , S.R. Sanders , V. Sathe , S. Naffziger and E. Alon, "A 32nm fully integrated reconfigurable switched-capacitor DC-DC converter delivering 0.55W/mm2 at 81% efficiency," *IEEE ISSCC 2010 Digest of Technical Papers*, February 7-11, 2010, pp. 210-211

[34] H. Meyvaert , T. Van Breussegem and M. Steyaert, "A monolithic 0.77W/mm2 power dense capacitive DC-DC step-down converter in 90nm Bulk CMOS," in *Proc. European Solid-State Circuits Conf. (ESSCIRC) 2011*, Sept. 12-16, 2011, pp. 486-486

[35] G. Villar Piqué, "A 41-phase switched-capacitor power converter with 3.8mV output ripple and 81% efficiency in baseline 90nm CMOS," *IEEE ISSCC 2012 Digest of Technical Papers*, February 19-23, 2012, pp. 98-100

[36] S. Bang, A. Wang, B. Giridhar, D. Blaauw, and D. Sylvester, "A fully integrated successive-approximation switched-capacitor DC-DC converter with 31mV output voltage resolution," *IEEE ISSCC 2013 Digest of Technical Papers*, February 17-21, 2013, pp. 370-371

[37] R. Jain, B. Geuskens, M. Khellah, *et al.*, "A 0.45–1V fully integrated reconfigurable switched capacitor step-down DC-DC converter with high density MIM capacitor in 22nm tri-gate CMOS," *Proc. IEEE Symposium VLSI Circuits*, June 12-14, 2013, pp. C174-175

[38] H.-P. Le, J. Crossley, S.R. Sanders, and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm2 at 73% efficiency," *IEEE ISSCC 2013 Digest of Technical Papers*, February 17-21, 2013, pp. 372-373

[39] A. Sarafianos and M. Steyaert, "The folding dickson converter: A step towards fully integrated wide input range capacitive DC-DC converters," in *Proc. European Solid-State Circuits Conf. (ESSCIRC) 2014*, Sept. 22-26, 2014, pp. 267-270

[40] J. Jiang, Y. Lu, C. Huang, *et al.*, "A 2-/3-Phase Fully Integrated Switched-Capacitor DC-DC Converter in Bulk CMOS for Energy-Efficient Digital Circuits with 14% Efficiency Improvement," *IEEE ISSCC 2015 Digest of Technical Papers*, February 22-26, 2015

[41] Y. Liu, J. Jiang, W.-H. Ki, *et al.*, "A 123-Phase DC-DC Converter-Ring with Fast-DVS for Microprocessors," *IEEE ISSCC 2015 Digest of Technical Papers*, February 22-26, 2015